Signal Integrity Optimization of MLVDS based Multi-master Instrument Bus

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Abstract— **In this paper, we proposed a MLVDS based multi-master real time instrument bus to simultaneously satisfy the requirement of high speed data transmission and low latency. A variety of approaches, such as characteristic impedance matching, termination matching, backplane layout design and isolation of MLVDS differential signals, are taken to optimize its signal integrity. Both the simulation and experiment results manifest that, the transmit rate of the proposed bus can reach 900Mbps (up to 1800Mbps).**

Keywords—signal integrity;multi-master instrument bus ; termination; simulation; high-speed

I. INTRODUCTION

Measuring and control systems are becoming increasingly complicated. Great majority of systems should utilize distributed system to cooperate fully with each other in order to accomplish one particular task, and sometimes may even call for high transmission rate as well as low latency. For example, as regard to data acquisition instrument system, there may be large amounts of raw data captured by various front-end acquisition modules to be transmitted for post processing, meanwhile, instructions from the processor (PC or the central control module) must be delivered immediately to make sure that the instrument work properly. Therefore, the instrument bus introduced for mutual communications between the internal modules becomes an important role in the instrument performance.

General Purpose Interface Bus (GPIB) is the first dedicated instrument bus, which is an 8-bit bus with only 8MB/s transfer rate [1-3]. The following instrument buses greatly improved the transmission rate, e.g. VXI (VME bus eXtensions for Instrumentation) up to 160MBps [4-5], PXI （PCI eXtension for Instrumentation） 264Mbps [6], PXI Express 6Gbps [7] and AXIe[8-9] (Advanced TCA Extensions for Instrumentation and Test) 320Gbps per link with extreme large size. The buses mentioned all above employ master-slave communication mode, i.e., a master-module is needed to coordinate the communication between the sub-modules. Although CAN [10] (Controller Area Network) and LXI (LAN-based eXtensions for Instrumentation) [11] can support multi-master communication, both cannot simultaneously satisfy the requirement of high data transmit rate and being real time.

MLVDS (Multipoint Low Voltage Differential Signaling) is an interface standard for multipoint applications with the date rate up to 500 Mbps, and has been successfully applied in different fields[12-14]. Multipoint operation allows for bidirectional communication over a single balanced media pair. We have proposed a novel instrument bus based on MLVDS (called MLVDS-based Multi-master Instrument Bus) [13], each module of which can launch a communication with other modules (in other words, every module can be the master module, say multi-master). A backplane is employed to interconnect the subsystem printed circuit boards through a series of connectors in the proposed bus.

With multiple pairs of high-speed signal in one connector and load changing along with the number of inserted modules, the backplane design is confronted with special challenges. At the speed of hundreds of Mbps, PCB traces behave like transmission lines and signal integrity can be degraded due to mismatches in the signal paths or incorrect terminations. The signal integrity of multi-master instrument bus (such as reflection, overshoot and undershoot, crosstalk and delay etc) has been attributed as the critical technique in the PCB design.

This paper focuses on optimizing signal integrity design of multi-master instrument bus to improve the overall transmission rate of the instrument, including the following two aspects: (1) analysis of factors affecting the signal integrity of multi-master instrument bus, and (2) methods adopted to optimize the design.

II. FACTORS AFFECTING SIGNAL INTEGRITY

A. Architecture of MLVDS-based multi-master instrument bus

The bus contains two physically separate but functionally similar transmission channels, .i.e. 8-bit massive data channel and 1-bit real-time message channel, both support multi-master communication. As the name suggests, the 8-bit massive–data channel is designed to transfer large data packets that may contains hundreds of bytes per packet, while the 1-bit timely-instruction channel for the short instruction (normally composed of several bytes) transmitted timely. Thanks to the dual-channel design, large packets and short instructions are transmitted independently. This means that the transmission of short instruction will not be delayed by the large packet, besides, the large packets will not be frequently interrupted by the instructions.

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As shown in Fig. 1, the MLVDS-based multi-master instrument bus system consists of multiple bus connectors, MLVDS transceivers, bus controllers (known as data link layer) that implemented on a FPGA(Field Programmable Gate Array) chip and optional CPUs (known as application layer) .

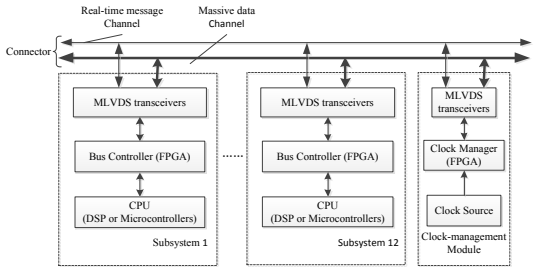


Fig. 1. Architecture of MLVDS-Based Multi-master Instrument Bus.

There are 12 subsystems (up to 32) and 1 clock-management module(different from the master card in VXI or PXI, and can be integrated into any card of the subsystems) in the bus design, that is, each MLVDS multipoint line contains 13 transceivers (SN65MLVD206D, made by TI).

The backplane and daughter boards are physically connected by the DIN41612 connectors. with subsystem 1 and subsystem12 cards inserted into slot1 and slot2, respectively, one pair of MLVDS differential signal flow can be described as Fig.2. To support the location of the various drivers throughout the transmission line, terminations are placed on both end-face of the backplane.

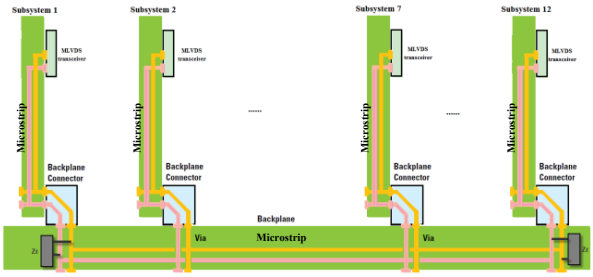


Fig. 2. Project of MLVDS-Based Multi-master Instrument Bus Simulation Model in Hyperlynx-Boardsim.

B. *Differential Transmission Line Characteristic Impedance*

As shown in Fig.2, a differential bidirectional high speed digital signal comes from one MLVDS transceiver, thus from the top/bottom layer to the backplane connectors, and reaches another MLVDS transceiver through the backplane board.

The structure of micro-strip is shown in Fig.3.

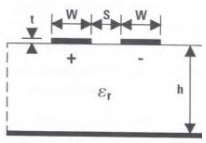


Fig. 3. Transmission Line Structure:microstrip.

Differential equivalent characteristic impedance of microstrip can be depicted as (1), and equivalent characteristic impedance of single-end line Z0 is depicted as (2).The "w" refers to the line width, "t" refers to thickness of copper(or other conductor), "s" refers to wire edge spacing, "h" refers to thickness of dielectric(often FR4) and "εr" refers to permittivity.

$$Z_{diff} = 2Z_0[1-0.48\exp(\frac{-0.96s}{h})](\Omega) \quad (1)$$

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln \frac{5.98h}{0.8w+t}(\Omega) \quad (2)$$

However, the impedance of transmission line is also affected by the load on the bus, for that every node can be seen as a capacitive load, thereby decreasing the impedance. The equivalent characteristic impedance with the loading terminations is called " effective characteristic impedance" in the following parts. The effective characteristic impedance can be calculated as (3).

$$Z_{diff}^{effective} = Z_{diff} \times \sqrt{\frac{c_0}{c_0 + N/\ell \times c_L}} \quad (3)$$

Z_{diff} refers to the differential equivalent characteristic impedance of microstrip, C0 (usually 2-3 pF/inch) refers to the equivalent capacitance of the transmission line per unit, $N/\ell \times c_L$ (usually 2.5 to 3.75 pF/inch) refers to the equivalent capacitance of the node, N refers to the number of nodes and refers to the length of signal line, c_L refers to the capacitance of one node.

As the effective characteristic impedance reduces, the signal loss increases and then the signal rise time decreases(means signaling rate decreasing). Therefore, when optimizing the signal integrity, not only should we control the characteristic impedance of micro-strip, but also curb effective impedance reducing.

C. *Backplane Connectors*

Backplane connector is one of the most important factors affecting the signal integrity. When the signal propagates from a controlled differential line to a unmatched connector, a signal reflection will be generated. Model of connector in high-speed transmission line can be simplified as RGLC, as shown in Fig.4.

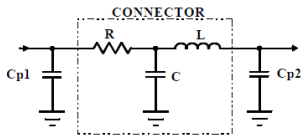


Fig. 4. Model of Connector.

Values of " R" , " C" and " L" can be obtained from the manufactures. As the length of connector increases, the equivalent value of " R" , " C", " L" increases, thereby decreasing the effective impedance and extending the transmission delay in the interior of the connector.

D. Backplane Impedance

As discussed above, both the node loads and backplane connectors can reduce the equivalent impedance of the bus. In the multi-point applications, as the number of communication node increases, the differential characteristic impedance of MLVDS transmission line is reduced.

In reference [15], a 21-slot, 8-layer backplane, equipped with the well-known DIN41612, 64-pin ac female connectors was chosen. And the Inductance-capacitance-resistance (the line impedance, Z0, the inductance, L0, and the capacitance, C0) measurements were made on the backplane as each daughter card was installed, as shown in Fig.5. As we can see, the inductance of backplane is relatively stable, but the capacitance is increasing with the increase of loads.

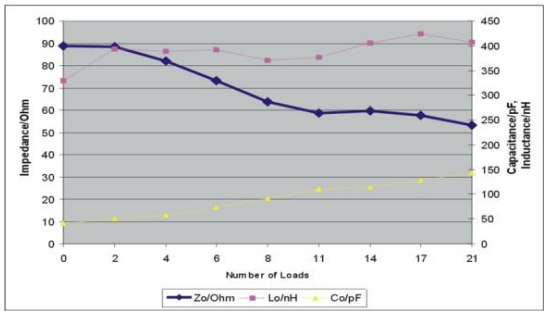


Fig. 5. Backplane Impedance as Daughter Cards Are Installed.

The connectors utilized in the backplane of MLVDS-based multi-master instrument bus is the same as in the reference [15], so we can estimate the backplane impedance from Fig. 5.

III. BACKPLANE DESIGN AND SIMULATION

The hardware circuit design is implemented on Protel99, and signal integrity simulation on Hyperlynx. The MultiBoard Project of MLVDS-based multi-master instrument bus simulation model is shown in Fig. 6. The simulation process can be simplified as:

(a) Transform .pcb (the format of PCB file in Protel99) files into .hyp (the format of file in Hyperlynx) files;

(b) Define board-to-board interconnect relationship and electrical characteristics;

(c) Setup the layer stack, mainly including the PCB lamination sequence and thickness which may be changed to meet the requirement of Impedance Control;

(d) Edit and validate the power network;

(e) Select the network to be simulated, and then load the corresponding IBIS models;

(f) Open digital oscilloscope and set the parameter of driving signal (Frequency, Mark-Space Ratio);

(g) Run the Simulation.

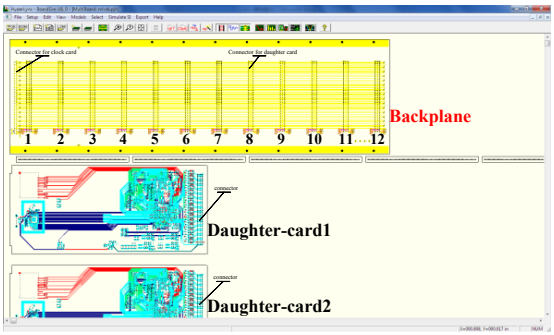


Fig. 6. The MultiBoard Project in Hyperlynx-Boardsim.

The following section will introduce the backplane circuit design and the corresponding simulation results.

A. Backplane Circuit Design

The system is based on electrical backplane circuit, which plays an important role in the signal integrity. Fig. 7 shows the schematic diagram of the backplane PCB layer stacks .

MLVDS differential line utilizes microstrip structure, and its differential impedance was controlled to 100 ohm. The backplane and daughter boards are physically connected by the DIN41612 connectors, where the signaling rate can be up to 200 Mbps. The distance between slots is set to 35.56mm.

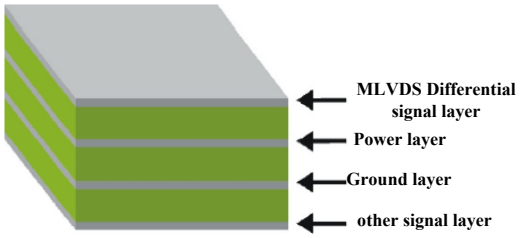


Fig. 7. Schematic Diagram of the Backplane PCBLayers.

B. *Electrical Characteristics of SN65MLVD206[16-17]*

SN65MLVD206D is multipoint-low-voltage differential (M-LVDS) line drivers and receivers, which is optimized to operate at signaling rates up to 200 Mbps.

The MLVDS standard defines a type 1 and type 2 receiver. Type 1 receivers include no provisions for failsafe and have their differential input voltage thresholds near zero volts. Type 2 receivers have their differential input voltage thresholds offset from zero volts to detect the absence of a voltage difference.

The driver of SN65MLVD206D has a differential output voltage magnitude of 480 mV to 650 mV, and the receiver of SN65MLVD206D is type 2, that detect the bus state with as little as 50 mV of differential input voltage over a common-mode voltage range of -1 V to 3.4 V.

Fig. 8 shown the available noise margin at the input of SN65MLVD206D .

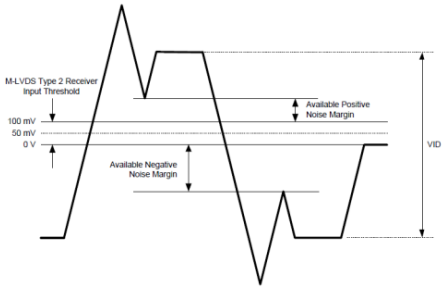


Fig. 8. Available Noise Margin to SN65MLVD206D Receiver.

C. *The Appropriate Terminating Resistor Value*

According to the Inductance-capacitance-resistance curve of backplane in Fig. 5 and (3) , we determined an approximate scope of termination resistance, and then analyzed the effect of termination resistor on noise margin by the eye pattern.

49.9 ohm, 54 ohm, 62 ohm, 68 ohm, 80 ohm and 100 ohm are selected to carry out a series of simulations to determine the most appropriate terminating resistance on a 12-node network in the case of fully loaded.

As shown in Fig. 9, the noise margin reaches the peak at the point of 62 ohm. Therefore, the resistor matching impedance is made of 62 ohm in the following simulation and experiment.

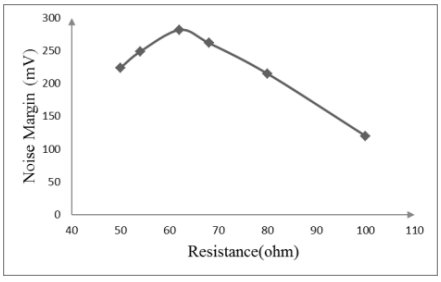
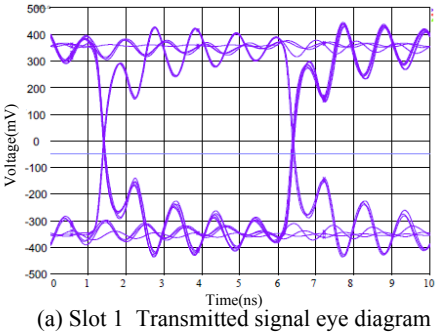


Fig. 9. Effect of Terminating Resistor on Noise Margin.

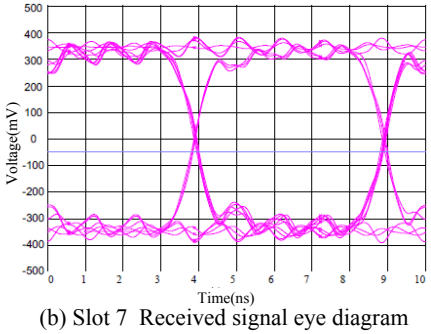
D. *Analysis of Signal Reflection*

To test the performance of signal reflection, slot1 as the driving node output a 200Mbps PBRS (Pseudo Random Binary Sequence) , and the whole nodes on the bus network receive the same signal. Fig.10 (a) (b) (c) are the eye pattern of the drive node(slot1 in Fig.6), intermediate node (slot7 in Fig.6) and the farthest node (slot12 in Fig.6) respectively viewed from the digital signal oscilloscope of Hyperlynx-Boardsim.

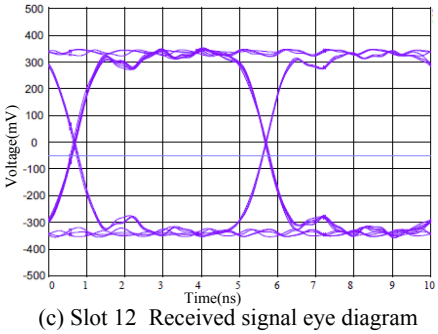
As shown in Fig.10, signal quality of slot1, which all the reflected signal from slot2 to slot 12 feed back to, is more poor with a terrible shock compared with other nodes. The farthest node's signal quality is better compared to other nodes because of the resistor, where the emission waveform can be well absorbed. But as the transmission distance increases, signal rise or fall time prolongs, and the signal amplitude declines to some extent.



(a) Slot 1 Transmitted signal eye diagram



(b) Slot 7 Received signal eye diagram



(c) Slot 12 Received signal eye diagram

Fig. 10. MLVDS Differential Signal Eye Diagrams of Simulation.

As can be seen in Fig.10, all the receiving signal can meet the requirement of MLVDS standard at the transmission rate of 200Mbps in spite of the worst signal reflection in slot1 .

IV. SIGNAL INTEGRITY TEST

In addition to the simulation, we have made a signal integrity test on the backplane board at full load. Fig.11 shows the MLVDS-based multi-master instrument bus entity with 12 loads.

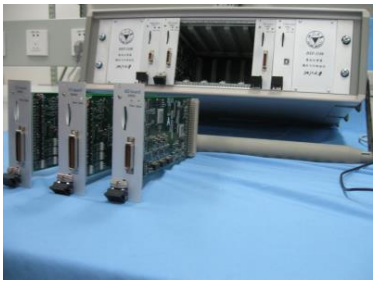
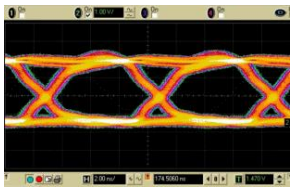
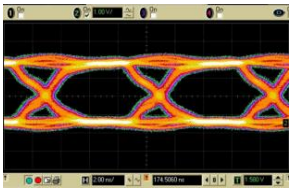


Fig. 11. MLVDS-based multi-master instrument bus entity.

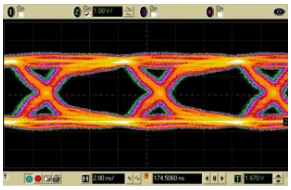
Similar to the Hyperlynx simulation, slot1 is the driving end with a (2^{15}-1) bit PBRS at the speed of 100MHz generated by a signal generator. The eye diagrams of received signals on slot1, slot2, slot7 and slot12 captured on an oscilloscope are shown in Fig.12.



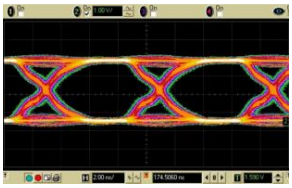
(a) Slot 1 Received signal eye diagram



(b) Slot 2 Received signal eye diagram



(c) Slot 7 Received signal eye diagram



(d) Slot 12 Received signal eye diagram

Fig. 12. Signal Eye Diagrams With the slot 1 as Signal Driving End.

Test results showed that, each MLVDS differential signal can be correctly received at the speed of 200Mbps. But considering the strategy of redundancy, the highest data transfer rate is set to 100Mbps in the real application.

V. CONCLUSION

MLVDS based multi-master instrument bus system employs a dual-channel structure, assisted by a high efficiency arbitration mechanism, can not only meet the need of high-speed and real-time communication, but also simplify the system structure by means of multi-master communication mechanism.

Thanks to all the efforts taken to optimize the signal integrity, including impedance control in transmission line, terminating resistor matching, PCB design of backplane and isolating of MLVDS differential signals, with the terminating resistor of 62 ohm, the transmit rate of the dual-channel can reach 100Mbps and 800Mbps respectively.

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